AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A drive circuit, comprising:

a plurality of digital-to-analog conversion circuits each of which selects one of difference reference voltages according ~~corresponding~~ to a digital gradation signal; and

a sampling circuit which selectively connects each output terminal of two of the digital-to-analog conversion circuits to signal lines,

wherein each of the digital-to-analog conversion circuits ~~between the selected reference voltage and the output terminal of the digital-to-analog conversion circuit~~ includes a variable resistor circuit with a resistance value corresponding to a digital gradation signal; and

wherein the sampling circuit comprises a plurality of pairs of switches, and a pair of switches is simultaneously activated and have an approximate same resistance value when the pair of switches is activated ~~switches each of which has an approximate same resistance value~~; and

wherein a divided voltage for outputting to a signal line ~~point of the selected reference voltages~~ is generated by a first series resistance and a second series resistance, the first resistance comprises a ~~comprising a resistance value of the~~ variable resistance circuit included in one of the digital-to-analog conversion circuits and one of the pair of switches, the one of the digital-to-analog conversion circuits is connected to the sampling circuit and the second series resistance comprises a variable resistor circuit included in another of the digital-to-analog conversion circuits and another of the pair of switches ~~a resistance value of the switches constituting the sampling circuit~~.

2. (Canceled)

3. (Currently Amended) A drive circuit, comprising:

a plurality of digital-to-analog conversion circuits each of which ~~connects~~ selects one of difference reference voltages corresponding to a digital gradation signal; ~~and~~

a plurality of variable resistor circuits with a resistance value corresponding to a digital gradation signal; and

a sampling circuit which selectively connects each output terminal of two of the ~~a plurality of~~ variable resistor circuits to one of a plurality of signal lines,

wherein each output terminal of the digital-to-analog conversion circuits connects to a corresponding variable resistor circuit; ~~with a resistance value corresponding to a digital gradation signal, and~~

wherein the sampling circuit comprises a plurality of pairs of switches, and a pair of switches is simultaneously activated and have an approximate same resistance value when the pair of switches is activated ~~switches each of which has an approximate same resistance value~~; and

wherein a divided voltage for outputting to a signal line ~~point of the selected reference voltages~~ is generated by a first series resistance and a second series resistance, the first series resistance comprises one of ~~comprising a resistance value of~~ the variable resistance circuits and one of the pair of switches, the one of the variable resistance circuits is connected to the sampling circuit and the second series resistance comprises another of variable resistor circuits and another of the pair of switches ~~a resistance value of the switches constituting the sampling circuit~~.

4. (Currently Amended) A drive circuit, comprising:

a plurality of digital-to-analog conversion circuits each of which outputs an analog signal corresponding to a digital gradation signal; ~~and~~

a plurality of variable resistor circuits with a resistance value corresponding to a digital gradation signal; and

a sampling circuit which selectively connects each output terminal of two of a plurality of variable resistor circuits to a corresponding one of ~~a plurality of~~ signal lines,

wherein each output terminal of the digital-to-analog conversion circuit connects to a corresponding variable resistor circuit ~~with a resistance value corresponding to a digital gradation signal~~,

wherein the sampling circuit comprises a plurality of pairs of switches, and a pair of switches is simultaneously activated and have an approximate same resistance value when the pair of switches are activated ~~switches each of which has an approximate same resistance value~~; and

wherein a divided voltage for outputting to a signal line ~~point of the selected reference voltages~~ is generated by a first series resistance and a second series resistance, the first resistance comprises one of ~~comprising a resistance value of the~~ variable resistance circuits and one of the switches, the one of variable resistance circuits is connected to the sampling circuit and ~~a resistance value of the switches constituting the sampling circuit~~ the second series resistance comprises another of variable resistor circuits and another of the pair of switches.

5. (Previously Presented) The drive circuit according to claim 3, wherein said plurality of variable resistor circuits include switching elements which conduct according to said gradation signal as the resistors with resistance values corresponding to said gradation signal.

6. (Previously Presented) The drive circuit according to claim 4, wherein said plurality of variable resistor circuits include switching elements which conduct according to said gradation signal as the resistors with resistance values corresponding to said gradation signal.

7. (Previously Presented) The drive circuit according to claim 3, wherein said plurality of variable resistor circuits include switching elements which conduct

according to said gradation signal and resistance elements, connected in series with each other, as the resistors with resistance values corresponding to said gradation signal.

8. (Previously Presented) The drive circuit according to claim 4, wherein said plurality of variable resistor circuits include switching elements which conduct according to said gradation signal and resistance elements, connected in series with each other, as the resistors with resistance values corresponding to said gradation signal.

9. (Currently Amended) A drive circuit, comprising:

a plurality of first digital-to-analog conversion circuits each of which selects one of difference positive reference voltages corresponding to a digital gradation signal;

a plurality of second digital-to-analog conversion circuits each of which selects one of difference negative reference voltages corresponding to a digital gradation signal; and

a sampling circuit which selectively connects each output terminal of two of the first digital-to-analog conversion circuits ~~and each output terminal of two of the second digital-to-analog conversion circuits~~ to signal lines,

wherein each of the first digital-to-analog conversion ~~circuit between the selected positive reference voltage and the output terminal of the digital-to-analog conversion~~ circuits includes a variable resistor circuit with a resistance value corresponding to a digital gradation signal;

wherein each of the second digital-to-analog conversion ~~circuit between the selected negative reference voltage and the output terminal of the digital-to-analog conversion~~ circuits includes a variable resistor circuit with a resistance value corresponding to [[a]] another digital gradation signal;

wherein the sampling circuit comprises a plurality of pairs of switches, a pair of switches is simultaneously activated and ~~each of which~~ has an approximate same resistance value when the pair of switches is activated; and

wherein a divided voltage for outputting a signal line is generated by a first series resistor and a second series resistor, the first resistor comprises a variable resistor circuit included in one of the first digital-to-analog conversion circuits and one of the pairs of switches, the one of the first digital-to-analog conversion circuits is connected to the sampling circuit and the second series resistor comprises a variable resistor circuit included in another of the first digital-to-analog conversion circuits and another of the pairs of switches;

wherein another divided voltage for outputting to another signal line is generated by a third series resistor and a fourth series resistor, the third series resistor comprises a variable resistor circuit included in one of the second digital-to-analog conversion circuit and one of the pair of switches, the one of the second digital-to-analog conversion is connected to the sampling circuit and the fourth series resistor comprises a variable resistor circuit included in one of the second digital-to-analog conversion circuit, the one of the second digital-to-analog conversion circuits is connected to the sampling circuit and the fourth series resistor comprises a variable resistor circuit included in another of the second digital-to-analog conversion circuits and another of the pairs of switches ~~point of the selected two of the positive reference voltages or a divided voltage point of the selected two of the negative reference voltages is generated on the signal lines by a series resistance comprising a resistance value of the variable resistance circuit and a resistance value of the switch constituting the sampling circuit~~.

10. (Canceled)

11. (Currently Amended) A drive circuit, comprising:

a plurality of first digital-to-analog conversion circuits each of which selects one of difference positive reference voltage ~~voltages~~ corresponding to a digital gradation signal;

a plurality of second digital-to-analog conversion circuits each of which selects one of difference negative reference voltage ~~voltages~~ corresponding to a digital gradation signal; ~~and~~

a plurality of first variable resistor circuits with a resistance value corresponding to a digital gradation signal;

a plurality of second variable resistor circuits with a resistance value corresponding to another digital gradation signal; and

a sampling circuit which selectively connects each output terminal of two of the first variable resistor circuits and each terminal of two of the second variable resistor circuits to signal lines,

wherein each output terminal of the first digital-to-analog conversion circuits connects to a corresponding first variable resistor circuit ~~with a resistance value corresponding to a digital gradation signal~~;

wherein each output terminal of the second digital-to-analog conversion circuits connects to a corresponding second variable resistor circuit ~~with a resistance value corresponding to a digital gradation signal~~,

wherein the sampling circuit comprises a plurality of pairs of switches, a pair of switches is simultaneously activated and ~~each of which~~ has an approximate same resistance value when the pair of switches is activated;

wherein a divided voltage for outputting to a signal line is generated by a first series resistor and a second series resistor, the first series resistor comprises one of the first variable resistor circuits and one of the pairs of switches, the one of the first variable resistor circuit is connected to the sampling circuit and the second series resistor circuit comprises another of the first variable resistor circuits and another of the pairs of switches; and

wherein another divided voltage for outputting to another signal line is generated by a third series resistor and a fourth series resistor, the third series resistor comprises one of the second variable resistor circuits and one of the pairs of switches, the one of the second variable resistor is connected to the sampling circuit and the fourth series resistor comprises another of the second variable resistor circuits and another of pairs of switches ~~point of the selected two of the positive reference voltages or a divided voltage point of the selected two of the negative reference voltages is generated on the signal lines by a series resistance comprising resistance value of the variable resistance circuit and a resistance value of the switches constituting the sampling circuit~~.

12. (Currently Amended) A drive circuit, comprising:

a plurality of first digital-to-analog conversion circuits each of which outputs a positive analog voltage corresponding to a digital gradation signal;

a plurality of second digital-to-analog conversion circuits each of which outputs a negative analog voltage corresponding to a digital gradation signal; ~~and~~

a plurality of first variable resistor circuits with a resistance value corresponding to a digital gradation signal;

a plurality of second variable resistor circuits with a resistance value corresponding to another digital gradation signal; and

a sampling circuit which selectively connects ~~in which~~ each output terminal of two of the first variable resistor circuits and each terminal of two of the second variable resistor circuits to ~~selectively connects each of two terminals of athe plurality of first variable resistor circuits and two terminals of athe plurality of second variable resistor circuits to a corresponding one of~~ signal lines,

wherein each output terminal of the first digital-to-analog conversion circuits connects to a corresponding first variable resistor circuit ~~with a resistance value corresponding to a digital gradation signal~~,

wherein each output terminal of the second digital-to-analog conversion circuits connects to a corresponding second variable resistor circuit ~~with a resistance value corresponding to a digital gradation signal~~,

wherein the sampling circuit comprises a plurality of pairs of switches, a pair of switches is simultaneously activated and ~~each of which~~ has an approximate same resistance value when the pair of switches is activated; ~~and~~

wherein a divided voltage for outputting to a signal line is generated by a first series resistor and a second series resistor, the first series resistor comprises one of the first variable resistor circuits and one of the pairs of switches, the one of the first variable resistor circuit is connected to the sampling circuit and the second series resistor circuit comprises another of the first variable resistor circuits and another of the pairs of switches; and

wherein another divided voltage for outputting to another signal line is generated by a third series resistor and a fourth series resistor, the third series resistor comprises one of the second variable resistor circuits and one of the pairs of switches, the one of the second variable resistor is connected to the sampling circuit and the fourth series resistor comprises another of the second variable resistor circuits and another of pairs of switches ~~point of the selected two of the positive reference voltages or a divided voltage point of the selected two of the negative reference voltages is generated on the signal lines by a series resistance comprising a resistance value of the variable resistance circuit and a resistance value of the switches constituting the sampling circuit~~.

13. (Previously Presented) The drive circuit according to claim 11, wherein said plurality of positive variable resistor circuits and said plurality of negative variable resistor circuits include switching elements which conduct according to said gradation signal as the resistors with resistance values corresponding to said gradation signal.

14. (Previously Presented) The drive circuit according to claim 12, wherein said plurality of positive variable resistor circuits and said plurality of negative variable resistor circuits include switching elements which conduct according to said gradation signal as the resistors with resistance values corresponding to said gradation signal.

15. (Previously Presented) The drive circuit according to claim 11, wherein said plurality of positive variable resistor circuits and said plurality of negative variable resistor circuits include switching elements which conduct according to said gradation signal and resistance elements, connected in series with each other, as the resistors with resistance values corresponding to said gradation signal.

16. (Previously Presented) The drive circuit according to claim 12, wherein said plurality of positive variable resistor circuits and said plurality of negative variable resistor circuits include switching elements which conduct according to said gradation signal and resistance elements, connected in series with each other, as the resistors with resistance values corresponding to said gradation signal.

17-21. (Canceled)

22. (Previously Presented) The drive circuit according to claim 4, wherein said switching elements comprise thin-film transistors.

23. (Previously Presented) The drive circuit according to claim 8, wherein said switching elements comprise thin-film transistors.

24. (Canceled)

25. (Previously Presented) The drive circuit according to claim 1, wherein said difference reference voltages are fewer in number than the gradations of displayed images.

26. (Canceled)

27. (Previously Presented) The drive circuit according to claim 3, wherein said difference reference voltages are fewer in number than the gradations of displayed images.

28. (Previously Presented) The drive circuit according to claim 4, wherein said difference reference voltages are fewer in number than the gradations of displayed images.

29. (Currently Amended) The drive circuit according to claim [[7]] 9, wherein said difference reference voltages are fewer in number than the gradations of displayed images.

30. (Canceled)

31. (Currently Amended) The drive circuit according to claim [[9]] 11, wherein said difference reference voltages are fewer in number than the gradations of displayed images.

32. (Currently Amended) The drive circuit according to claim [[10]] 12, wherein said difference reference voltages are fewer in number than the gradations of displayed images.

33. (Original) An image display apparatus equipped with the drive circuit according to claim 1, wherein a plurality of signal lines for transmitting image signals and a plurality of scanning lines for transmitting scanning signals are formed in a matrix-like fashion in an image display area of a substrate, an electro-optical conversion element which changes its light transmittance or emission intensity in response to an electrical signal is placed near each intersection of the signal lines and scanning lines on said substrate, said signal lines are connected to said drive circuit, and said scanning lines are connected to a scanning circuit.

34. (Canceled)

35. (Original) An image display apparatus equipped with the drive circuit according to claim 3, wherein a plurality of signal lines for transmitting image signals and a plurality of scanning lines for transmitting scanning signals are formed in a matrix-like fashion in an image display area of a substrate, an electro-optical conversion element which changes its light transmittance or emission intensity in response to an electrical signal is placed near each intersection of the signal lines and scanning lines on said substrate, said signal lines are connected to said drive circuit, and said scanning lines are connected to a scanning circuit.

36. (Original) An image display apparatus equipped with the drive circuit according to claim 4, wherein a plurality of signal lines for transmitting image signals and a plurality of scanning lines for transmitting scanning signals are formed in a matrix-like fashion in an image display area of a substrate, an electro-optical conversion element which changes its light transmittance or emission intensity in response to an electrical signal is placed near each intersection of the signal lines and scanning lines on said substrate, said signal lines are connected to said drive circuit, and said scanning lines are connected to a scanning circuit.

37-40. (Canceled)

41. (Currently Amended) An image display apparatus equipped with the drive circuit according to claim [[7]] 9, wherein a plurality of signal lines for transmitting image signals and a plurality of scanning lines for transmitting scanning signals are formed in a matrix-like fashion in an image display area of a substrate, liquid crystals which change their light transmittance in response to an electrical signal are placed near each intersection of the signal lines and scanning lines on said substrate, said liquid crystals are sandwiched between said substrate and another substrate, said

signal lines are connected to said drive circuit, and said scanning lines are connected to a scanning circuit.

42. (Canceled)

43. (Currently Amended) An image display apparatus equipped with the drive circuit according to claim [[9]] 11, wherein a plurality of signal lines for transmitting image signals and a plurality of scanning lines for transmitting scanning signals are formed in a matrix-like fashion in an image display area of a substrate, liquid crystals which change their light transmittance in response to an electrical signal are placed near each intersection of the signal lines and scanning lines on said substrate, said liquid crystals are sandwiched between said substrate and another substrate, said signal lines are connected to said drive circuit, and said scanning lines are connected to a scanning circuit.

44. (Currently Amended) An image display apparatus equipped with the drive circuit according to claim [[10]] 12, wherein a plurality of signal lines for transmitting image signals and a plurality of scanning lines for transmitting scanning signals are formed in a matrix-like fashion in an image display area of a substrate, liquid crystals which change their light transmittance in response to an electrical signal are placed near each intersection of the signal lines and scanning lines on said substrate, said liquid crystals are sandwiched between said substrate and another substrate, said signal lines are connected to said drive circuit, and said scanning lines are connected to a scanning circuit.

45. (Previously Presented) The image display apparatus according to claim 41, wherein said switching elements comprise thin-film transistors.

46. (Canceled)

47. (Previously Presented) The image display apparatus according to claim 43, wherein said switching elements comprise thin-film transistors.

48. (Previously Presented) The image display apparatus according to claim 44, wherein said switching elements comprise thin-film transistors.

49. (Previously Presented) The image display apparatus according to claim 41, wherein said reference voltages are fewer in number than the gradations of displayed images.

50. (Canceled)

51. (Previously Presented) The image display apparatus according to claim 43, wherein said reference voltages are fewer in number than the gradations of displayed images.

52. (Previously Presented) The image display apparatus according to claim 44, wherein said reference voltages are fewer in number than the gradations of displayed images.